

- So there always exist at least two middle switches through which there are paths from any given input switch to all the output switches. Since the number of middle switches $m = 2 * n$ is sufficient to set up the multicast connections, the $V(m, n, r)$ Clos network can be operated in rearrangeably nonblocking manner. Hence, if $m \geq 2 * n$, the
- 5 $V(m, n, r)$ Clos network can be operated in rearrangeably nonblocking manner for multicast connections of any arbitrary fan-out.

- Now the proof that the $V(m, n, r)$ network is strictly nonblocking for multicast assignments when $m = 3 * n - 1$ is presented. Compared to strictly nonblocking unicast algorithm, in the above provided proof for rearrangeably nonblocking where $m \geq 2 * n$
- 10 applicant notes that for realizing a multicast connection from each inlet link in an input switch, one additional potential first internal link is taken away from the rest of the inlet links from the same input switch and hence with an additional $n - 1$ middle switches, one each for the first $n - 1$ inlet links, the $V(m, n, r)$ network is strictly nonblocking for multicast assignments.

- 15 To extend the proof (described above), applicant now shows that $V(m, n_1, r_1, n_2, r_2)$ network can be operated in rearrangeably nonblocking manner for multicast connections when $m \geq n_1 + n_2$, by considering the two cases $n_1 < n_2$ and $n_1 > n_2$.

- 20 1) $n_1 < n_2$: In this case, the number of middle switches necessary is $2 * n_1$ which is $< (n_1 + n_2)$. To prove the sufficiency, even though there are a total of $n_2 * r_2$ outlet links in the network, in the worst-case scenario only $n_1 * r_2$ second internal links will be needed. This is because, even if all $n_2 * r_2$ outlet links are destinations of the connections, using the fan-out capability in the output switches the rearrangeably nonblocking behavior can be realized. And so $2 * n_1$ which is $< (n_1 + n_2)$ middle switches is
- 25 sufficient.

2) $n_1 > n_2$: In this case, since there are a total of $n_2 * r_2$ outlet links in the network, only a maximum of $n_2 * r_2$ second internal links will be used even if all the $n_2 * r_2$ outlet links are destinations of the network connections. When the number of

middle switches is $n_1 + n_2$ the total second internal links in the network is given by $r_2 * (n_1 + n_2)$ which is more than the required number, according to the rearrangeability proof for $V(m, n, r)$ as shown earlier, which is $r_2 * (2 * n_2)$. Also from any input switch only a maximum of n_2 out of n_1 available inlet links can each have fan-out of r_2 . And so only a maximum of n_2 connections from any input switch need to be fanned out into two. And so $n_1 + n_2$ middle switches are sufficient.

The extension of the proof when $m \geq 2 * n_1 + n_2 - 1$ that $V(m, n_1, r_1, n_2, r_2)$ network is operated in strictly nonblocking manner, is similar to that of $V(m, n, r)$ network.

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Table 3
A multicast assignment in a $V(14,5,25)$ Network

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Requests for $r = 1$	Requests for $r = 2$	Requests for $r = 3$
$I_1 = \{1, 2, 3, 4, 5\},$	$I_6 = \{1, 6, 11, 16, 21\},$	$I_{11} = \{1, 7, 13, 19, 25\},$
$I_2 = \{6, 7, 8, 9, 10\},$	$I_7 = \{2, 7, 12, 17, 22\},$	$I_{12} = \{2, 8, 14, 20, 21\},$
$I_3 = \{11, 12, 13, 14, 15\},$	$I_8 = \{3, 8, 13, 18, 23\},$	$I_{13} = \{3, 9, 15, 16, 22\},$
$I_4 = \{16, 17, 18, 19, 20\},$	$I_9 = \{4, 9, 14, 19, 24\},$	$I_{14} = \{4, 10, 11, 17, 23\},$
$I_5 = \{21, 22, 23, 24, 25\},$	$I_{10} = \{5, 10, 15, 20, 25\},$	$I_{15} = \{5, 6, 12, 18, 24\},$
Requests for $r = 4$	Requests for $r = 5$	
$I_{16} = \{1, 8, 15, 17, 24\},$	$I_{21} = \{1, 9, 12, 20, 23\},$	
$I_{17} = \{2, 9, 11, 18, 25\},$	$I_{22} = \{2, 10, 13, 16, 24\},$	
$I_{18} = \{3, 10, 12, 19, 21\},$	$I_{23} = \{3, 6, 14, 17, 25\},$	
$I_{19} = \{4, 6, 13, 20, 22\},$	$I_{24} = \{4, 7, 15, 18, 21\},$	
$I_{20} = \{5, 7, 14, 16, 23\},$	$I_{25} = \{5, 8, 11, 19, 22\}$	

Table 3 shows an exemplary multicast assignment in a $V(10,5,25)$ network. Each request has a fan-out of five. All the outlet links are connected in this multicast assignment since each output switch is used exactly five times in the requests corresponding to five outlet links of each output switch. In one implementation, Table 4 shows by using only $m = 3 * n - 1 = 14$ middle switches, the multicast assignment can be set up to operate the network in strictly nonblocking manner.

TABLE 4
A strictly nonblocking Schedule of the
Multicast assignment of Table 3

	M = 1	M = 2	M = 3	M = 4	M = 5	M = 6	M = 7
R=1	1,2	3,4,5	6,7	8,9,10	11,12	13,14,15	16,17
R=2	6,11,16,21	1	2,12,17,22	7	3,8,13,18,23	4,9,19,24	14
R=3	7,13,19,25	2, 8,14,20,21	1	3,15,16,22	9	10,11,17,23	4
R=4	8,15,17,24	9,11,18,25	3,10,19,21	1	2	12	6,13,20,22
R=5	9,12,20,23	10,13,16,24	14,25	2	1	7,18,21	5,8,11,19

	M = 8	M = 9	M = 10	M = 11	M = 12	M = 13	M = 14
R=1	18,19,20	21, 22	23,24,25				
R=2	5,10,15,25	20					
R=3	6,12,24	5,18					
R=4	4	7,14,16,23	5				
R=5	22	3,6,17	4,15				

Each row in Table 4 represents an input switch and each column represents a middle switch. And each element in the table represents the list of output switches set up through the corresponding middle switch for a connection originating from the corresponding input switch. The correspondence between different connections from the same row of Table 4 and hence from the same input switch can be obtained from the multicast assignment of the Table 3.

Referring to FIG. 5A a five stage strictly nonblocking network is shown according to an embodiment of the present invention that uses recursion as follows. The five stage network comprises input stage 110 and output stage 120, with inlet links IL1-IL12 and outlet links OL1-OL12 respectively, where input stage 110 consist of six, two by five switches IS1-IS6, and output stage 120 consist of six, five by two switches OS1-OS6. However, unlike the single switches of middle stage 130 of the three-stage network of FIG. 1A, the middle stage 130 of FIG. 5A consists of five, six by six three-stage subnetworks MS1-MS5 (wherein the term "subnetwork" has the same meaning as the term "network"). Each of the five middle switches MS1-MS5 are connected to each of